VMEbus FAQ- Frequently Asked Questions for the Beginning VMEbus User

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Question: Recently I've been hearing about new high performance VME backplanes. How are they different from traditional VME backplanes and how will they enhance VME performance?

Introduction- The VMEbus backplane provides the transport media for electrical signals between modules. As originally defined a VME backplane can contain up to 21 slots. Why was 21 slots selected? Because if you space connectors at 0.8 inch you can just get 21 slots into a chassis which will fit into a 19 inch rack. Backplanes can contain less than 21 slots and sizes such as 5, 7, 9, 12, and 15 slots are popular. For really small systems even 3 slot backplanes can be used.

The VMEbus defines an asynchronous backplane protocol which uses handshaking signals rather than a clock to transfer data. Since the backplane is viewed as a transmission line, certain time delays are defined to assure that signals reach a known state before they are deemed valid. These time delays were determined by taking into account a fully loaded 21 slot backplane and characteristics of specific TTL logic available when the VMEbus was developed in the early 1980s.

These delays have stood the test of time and have provided reliable operation for VMEbus systems in a variety of configurations and applications.

VME320- At the January 1997 Real Time Computer Show in Santa Clara, CA. a revolutionary announcement was made. Drew Berding, Arizona Digital, displayed a 21 slot VMEbus backplane that could transfer data at a 320 Mbyte/second data rate. His demonstration was even more dramatic because one of the modules was on a standard extender board. Scope traces showed the signals to be very clean even though signals were running from slot 1 to slot 21 and then through an extender board in a fully loaded system.

Much speculation ensued as to how the backplane was constructed. While many ideas were put forth, the method employed by Drew was both elegant and straightforward. A standard backplane trace goes from slot 1 to slot 2 to slot 3 and so on through slot 21. In the VME320 backplane each slot trace is wired directly to slot 11 in a basic star configuration so that a signal from slot 1 to slot 2 goes from slot 1 to slot 11 and then back to slot 2. Wiring the backplane in this manner changes the backplane signal characteristics dramatically. Instead of looking like a transmission line, the VME320 backplane looks like a lumped capacitance. As a result signal lines are cleaner, noise is reduced, and data transfer rates can be effectively increased.

While Drew's announcement created a lot of interest from users, it also caused the VMEbus community to revisit the original assumptions for backplane design and to see what other design changes could be made to enhance backplane performance.

A Second Look- At the March 1998 VSO meeting in Geneva, Switzerland, Andreas Lenkisch, Trenew, presented research he had done to enhance backplane performance in a paper titled; ***VME Breaks Performance Barrier Again - 1000 Mbytes/s Range Possible***. In the paper he noted that a reduction in trace impedance improved signal waveforms and might allow higher speed transfers in a traditional stitched backplane.

In May, Bob Sullivan, Hybricon, presented work he had to done showing the possiblity of moving data at 560 Mbytes/sec with existing ABTE ETL transceivers. Hybricon's approach was to use diode terminations and a modified bus topology to increase the effective impedance of the backplane.

The battle of the backplanes continued at the July VSO meeting where Andreas Lenkisch, Trenew, presented additional results to the approach he had proposed in March and Drew Berding, Arizona Digital, compared the various approaches and presented arguments regarding the advantages of the star backplane approach.

Drew's original announcement in January 1997 has unleased new research into backplane characteristics and has spurred many companies to reconsider the way backplanes are built.

2eSST- To take advantage of these new backplane technologies, the VITA Standards Organization (VSO) set up a task group early in 1997 to begin work on a new protocol. The task group decided to specify a synchronous protocol that would provide data transfer rates of 320 Mbytes/second and greater.

The 2eSST protocol, is based on the asynchronous 2eVME protocol. The main exception to this is that during its data phases, 2eSST is a source synchronous protocol. No acknowledgment is expected from the receiver of the data. Hence, the theoretical performance of 2eSST is limited only by the skew between receiver and transmitter of data. Like 2eVME it uses incident wave switching to guarantee fast switching times and minimize skew. The result is a protocol that as currently defined doubles the theoretical bandwidth of VME to 320Mbytes/sec. The protocol can be broken into three main phases: address broadcast, data phase and termination.

The address broadcast phase for 2eSST is identical to the address broadcast phase for 2eVME. However, the data phase is synchronous rather than asynchronous.

Traditional VME utilizes a handshake protocol whereby data strobes (DS1* and DS0*) are acknowledged by DTACK* which then allows the data strobes to be removed which in turn allows the DTACK* to be removed. Once DTACK* is deasserted, a new cycle can begin.

Traditional VME protocol requires four delays through the drivers, backplane and receivers plus the settling time of the backplane. 2eVME protocol

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found in three devices, the single bridge ASIC allows placement of more functionality on a single board computer. The MVME2400 supports 32 to 256 MB of ECC SDRAM. Other features include 10/100Mb Ethernet, two PCI Mezzanine Card (PMC) slots with front panel and P2 I/O, one serial port and 9MB of onboard FLASH. The MVME2400 is scheduled for January 1999 production availability. Motorola Computer Group is on the web at; www.mcg.mot.com/

Myriad Logic Inc. has announced the FC-2930/R, a high performance dual port fibre channel interface for the Mercury RACE Series VME and Mulitport 9U four-port motherboards. The double-deep daughtercard has two l-Gigabit/second fiber optic connections for high-bandwidth arbitrated loop, point-to-point. or switched topology networking. Designed to interconnect high-throughput realtime systems, RAIDs and general-purpose computers, the FC-2930/R is built to sustain 180 Mbytes/second, 90 Mbytes/second per channel, throughput to disk arrays and for peer-to-peer comunications. Myriad Logic is on the web at; www.myriadlogic.com

North Atlantic Instruments, Inc. has introduced the new VME 5410-158 with up to 32 low side, high current, solid state opto-isolated switched outputs with diagnostics. The single-slot VMEbus card incorporates short circuit and transient protection, switch readback rate, and has a drive capability of 2 amps continuous @ 85° C. The VME 5410-158 is available in 16, 24, and 32 channel versions with short circuit and transient protection as well as open circuit, short circuit, over temperature, fault and overload detection. All VME digital lines and power are opto-isolated from switched external power. North Atlantic is on the web at; www.naii.com/

Peritek Corp. announces the immediate availability of a powerful new PMC (PCI Mezzanine Card) graphics generator for the VMEbus and CompactPCI embedded markets. The Model VFX-M brings a 128-bit graphics engine to the PMC bus. Utilizing the Number Nine 1128 2D/3D graphics engine, it combines VGA compatibility and unmatched performance with a flexible graphics interface which can cover a wide range of 8, 16, and 24-bit display applications. Peritek is on the web at; www.peritek.com.

Systran Corp. has introduced the FibreXpress Simplex Link, a system that allows Front Panel Data Port (FPDP) connections to be extended over distances up to l0 km. The Simplex Link maintains the simplicity, high-bandwidth and low latency of FPDP connections, while supporting long-distance and multiple destination broadcast capabilities. The Simplex Link is implemented by sets of Simplex Link Source Cards (SLSCs) and corresponding Simplex Link Destination Cards (SLDCs). In a standard point-to-point configuration, all data is transmitted from a single Source Card to a single Destination Card, and the Destination Card can provide flow control commands back to the Source Card. Systran is on the web at; www.systran.com

VMETRO has announced a new member of its popular Bus Analyzer family: The PBTC-415 CompactPCI Bus Analyzer & Exerciser. With its sampling speed up to 66.7MHz, optionally 400MHz, built-in Exerciser and optional Anomaly Trigger, it is the fastest and most comprehensive CompactPCI bus analyzer on the market. Designed for debugging and verification of next-generation CompactPCI board and system designs, the PBTC-415 PCI Bus Analyzer & Exerciser is a single-slot 3U card that contains a complete logic analyzer and exerciser for the CompactPCI bus. VMETRO is on the web at; www.vmetro.com

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PVIC MirroredMemory (MM)

The PVIC implements a local read and global write Mirrored Memory concept. The first part of the MM is reserved for the write and read buffers of the PVIC system. The rest is available for the user. Apart from the previously mentioned PVIC message FIFO for efficient interrupt dispatching, it also implements a global reservation mechanism. This mechanism allows the implementation of hardware semaphores, test-and-set operations and other atomic operations in a flexible and efficient way. This feature was especially added for distributed processing, farming etc.

PVIC Implementations

The following PVIC products are available:

PVIC8426	CES RIO8062 [2] - PVIC Interface with PVIC Bridge.
PVIC8425	PMC-PVIC single slot PMC with embedded GTL+ physical interface.
PVIC4025	CompactPCI - PVIC System Slot or Peripheral Slot (3U and 6U versions).
PVIC7225	PCI - PVIC 32-bit 33 MHz.
PVIC8025	VME64x - PVIC interface with PVIC Bridge.
PIB6800	GTL+ 0.025" ribbon flat cable, up to 2 meters at 66 MHz.
PIB6801	Differential Interface, 68pin SCSI cable type, up to 15m at 66MHz or 30m at 33 MHz.
PIB6802	Optical Link up to 200 meters, 1.4 Gbit/s.

PVIC System Example

Figures 6 and 7 (page 14) show two typical PVIC system examples. It is possible to mix PVIC DIFF with PVIC GTL+ through bridge elements. The PVIC bridge is only translating the electrical levels. The PVIC protocol remains identical and the system remains completely transparent.

REFERENCES
[1] CES, PVIC 8426 Technical Specification.
[2] CES, RIO2 8062 User's Manual. DOC 8062/UM ver 1.0, Oct 1997.

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improves upon this by using both edges of DS1*, DS0*, and DTACK* to qualify data. Throughput is doubled, but performance is still limited by the requirement for acknowledgment from the receiver of data.

In contrast, after the address phase, the 2eSST protocol sends the data and strobe and does not wait for any acknowledgments. Therefore, data can be sent at much higher bandwidth. Both edges of the strobe are used: falling edge for odd data beats and rising edge for even data beats.

SUMMARY- Over time the VMEbus has evolved to meet new requirements. With the announcement in January 1997 of higher performance backplanes, a new wave of VME performance improvements has begun that will allow users to meet the demanding data applications of the 21st century.